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wherein the size of said second low impurity concentration diffusion layer formed on the surface of the semiconductor substrate, which extends from said second gate to reach said second high impurity concentration diffusion layer, is larger than the size of said first low impurity concentration diffusion layer formed on the surface of the semiconductor substrate, which extends from said second gate to reach said second high impurity concentration diffusion layer, and a lower end of an outer surface of the second gate side wall being positioned within a surface region of the second low impurity concentration diffusion layer apart from an interface between the second low impurity concentration diffusion layer and the second high impurity concentration diffusion layer.

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#### REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-7 are presently active in this case. Claims 8-18 stand withdrawn from consideration. The present amendment amends Claim 1. The above amendment shows the amended claims in clean form, the attachment shows a marked-up copy for the Examiner's convenience.

In the outstanding Office Action, Claims 3 and 5-7 were rejected under 35 U.S.C. § 112, first paragraph. Claims 1-2 and 4 were rejected under 35 U.S.C. § 102(b) as anticipated by Kang et al. (U.S. Patent No. 5,278,441). Claims 1 and 4 were rejected under 35 U.S.C. § 102(e) as anticipated by Applicants Admitted Art (pages 1-11, Figs. 21-22).

In response to the rejection of Claims 3 and 5-7 under 35 U.S.C. § 112, first paragraph, Applicants submit that the subject matter described in Claims 3 and 5-7 is fully described in the elected embodiment.

Applicants respectfully submit that all device Claims 1-7 are also directed to the non-elected species of Figs. 1-11. The specification states "Incidentally, the low voltage PMOS transistor and the low voltage NMOS transistor are formed by the method similar to that employed in the first embodiment and, thus, the description with reference to the drawing is omitted here".<sup>3</sup> Moreover, Applicants' also note specification states "Incidentally, the construction of the low voltage PMOS and NMOS transistors are equal to those in the first embodiment".<sup>4</sup> Further, the subject matter of Claims 3 and 5-7 is fully described in Figs. 2 and 4A-9B. In such ways, Applicants submit that Figure 9B and the corresponding description show a corresponding structure of low voltage transistors for the embodiment in which high voltage transistors are shown in Figures 13-20. Therefore, Claims 3 and 5-7 are believed to be fully supported by the specification and drawings in light of their inclusion by reference in the selected embodiment.

In response to the rejections to Claims 1-2 and 4 under 35 U.S.C. § 102(b) in view of Kang et al. and Claims 1 and 4 under 35 U.S.C. § 102(e) in view of the admitted art, those rejections are traversed by the present response.

Kang et al. shows in Fig. 5G that the widths of the first source and drain 83, 84 of the PMOS transistor are wider than those of the first source and drain 80, 81 of the NMOS transistor. However, as seen in Fig. 5G, in the PMOS transistor, the interfaces between the ion-implanted regions 83, 98 and 84, 99 correspond to lower edges of outer surfaces on the first gate side walls 86 and 94. Further, applicants note that the upper edge of the first gate side wall 86 as well as that of the first gate side wall 94 are terminated at the top edge of the second gate 76 to expose the upper surface of the second gate 76.

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<sup>3</sup> Specification at page 46, line 27, to page 47, line 4.

<sup>4</sup> Specification at page 42, lines 19-21.

In contrast to Kang et al., according to the structure shown in Fig. 13 as a non-limiting example, only the first gate side wall 10 of the PMOS transistor 75 has an upper edge terminating at the top edge of the gate electrode 13 and the film 82 acting as a second gate side wall covering the top surface of the gate electrode 13, in contrast to the second gate side wall 94 shown in Kang et al.

The first and second gate side walls 86 and 94 in Kang et al. correspond to the first gate side wall 10 as shown in Fig. 13 of the present application. The lower end of the outer surface of the first gate side wall 10 is positioned within a surface region of the low impurity concentration diffusion layers 77a, 77b apart from the interface between the low impurity concentration diffusion layers 77a, 77b and the high impurity concentration diffusion layers 76a, 76b, as again shown in Fig. 13 as a non-limiting example.

According to that structure of Fig. 13 of the present specification, since the lower edge of the gate side wall 10 is positioned closer to the gate electrode 13 than the interface between the low impurity concentration diffusion layers 77a, 77b and the high impurity concentration diffusion layers 76a, 76b, and since the gate side wall 82 does not have the lower edge facing the interface of the layers 76a, 76b and 77a, 77b, unlike the structure in Kang et al. as shown in Fig. 5G, it is possible to reduce the cell size or to at least have a sufficient tolerance for the formation of the contact plug. In other words, in the present invention it is possible to suppress the short channel effect and to decrease the distance between the contact plug and the gate electrode in the peripheral transistor and the memory cell transistor to decrease the pattern size.<sup>5</sup>

Claim 1 has been amended to recite the above structure. As such a structure recited in Claim 1 is not taught or suggested by Kang et al., thus Claim 1 distinguishes over Kang et al.

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<sup>5</sup> Specification at page 49, lines 1-14.

Further, the above-noted recited and clarified structure in Claim 1 is also neither taught nor suggested in the admitted art, and thus Claim 1 also distinguishes over the admitted art.

Claims 2 and 4 in light of their dependency to Claim 1 are also believed to be patentable over the cited references. Thus, in light of the above amendments to Claim 1, all the rejections under 35 U.S.C. § 102 are believed to be overcome.

Consequently, in view of the present amendment, no further issues are believed to be outstanding in the present application, and the present application is believed to be in condition for formal allowance. A notice of allowance for Claims 1-7 is earnestly solicited.

Should the Examiner deem that any further action is necessary to place this application in even better form for allowance, he/she is encouraged to contact Applicants' undersigned representative at the below-listed telephone number.

Finally, the attention of the patent office is directed to the change of address of Applicants' representative, effective January 6, 2003:

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Please direct all future communications to this address.

Respectfully submitted,

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IN THE SPECIFICATION

Page 42, lines 11-21, please replace the paragraph as follows:

--In other words, the effective channel length is further increased by the shortening of the LDD length 94, compared with the first embodiment, leading to improvements in the punch-through breakdown voltage and in the short channel effect. Alternatively, since it is possible to decrease the length of the gate electrode 13, it is possible to decrease the formation area of the transistor 75, compared with the conventional high voltage PMOS transistor. Incidentally, the construction of the [high] low voltage PMOS and NMOS [transistor 4 is] transistors are equal to [that] those in the first embodiment.--

IN THE CLAIMS

--1. (Amended) A semiconductor device, comprising:

a first transistor including a first gate formed on a semiconductor substrate, a first low impurity concentration diffusion layer formed on the surface of said semiconductor substrate in a manner to surround said first gate, a first high impurity concentration diffusion layer formed on the surface of the semiconductor substrate in a manner to surround said first low impurity concentration diffusion layer, and a first gate side wall formed to surround the first gate with a top surface of the first gate being exposed from an upper end of the first gate side wall, and an interface between the first low impurity concentration diffusion layer and the

first high impurity concentration diffusion layer corresponding to a lower end of an outer surface of the first gate side wall; and

a second transistor including a second gate formed on the semiconductor substrate, a second low impurity concentration diffusion layer formed on the surface of the semiconductor substrate in a manner to surround said second gate, a second high impurity concentration diffusion layer formed on the surface of the semiconductor substrate in a manner to surround said second low impurity concentration diffusion layer, and a second gate side wall formed to surround said second gate and having a thickness equal to that of the first gate side wall of said first transistor, a top surface of the second gate being exposed from an upper end of the second gate side wall;

wherein the size of said second low impurity concentration diffusion layer formed on the surface of the semiconductor substrate, which extends from said second gate to reach said second high impurity concentration diffusion layer, is larger than the size of said first low impurity concentration diffusion layer formed on the surface of the semiconductor substrate, which extends from said second gate to reach said second high impurity concentration diffusion layer, and a lower end of an outer surface of the second gate side wall being positioned within a surface region of the second low impurity concentration diffusion layer apart from an interface between the second low impurity concentration diffusion layer and the second high impurity concentration diffusion layer.--